REMARKS

Claims 1, 4-5, 7, 10 and 13-14 are now pending in the application. Applicant amends claims 1, 4-5, 7 and 10, cancels claims 3, 6 and 15. Support for the amendments can be found throughout the specification, claims and drawings as originally filed. Accordingly, no new matter is added. Applicant respectfully requests reconsideration and withdrawal of the rejections in view of the amendments and remarks contained herein.

REJECTION UNDER 35 U.S.C. § 112

Claim 6 stands rejected under 35 U.S.C. § 112, first paragraph, as failing to comply with the written description requirement. This rejection is respectfully traversed. Notwithstanding Applicant's traverse and solely in the interest of expediting prosecution, Applicant cancels claim 6. Accordingly, this rejection is moot.

REJECTION UNDER 35 U.S.C. § 102

Claims 1, 3-5, 10, 13-14 and 15 stand rejected under 35 U.S.C. § 102(b) as being anticipated by Kobayashi et al. (U.S. Pat. No. 6,489,649). This rejection is respectfully traversed. Notwithstanding Applicant's traverse and solely in the interest of expediting prosecution, Applicant amends independent claim 1.

Amended claim 1 recites a semiconductor device comprising: a base including a semiconductor material, the base having a source region, a drain region and a channel region disposed between the source region and the drain region; a gate insulating material disposed in contact with the channel region of the base; and a

gate electrode disposed on the gate insulating material. The gate insulating material includes silicon, oxygen, either hydrogen or deuterium, and at least one other element. The gate insulating material has a first region where B/A is 10 or less, where a concentration of the at least one other element in the first region is defined as A, and a concentration of the hydrogen or deuterium in the first region is defined as B. The gate insulating material has a second region where D/C is 1.6 or more, where a concentration of the at least one other element in the second region is defined as C, and a concentration of the hydrogen or deuterium in the second region is defined as D. The second region is located at a portion of the gate insulating material at a distance in a thickness direction of Y/10 of the gate insulating material from an interface between the channel region of the gate insulating material and the base, where Y is an average thickness of the gate insulating material.

Thus, claim 1 recites that **the gate insulating material has a second region where C and D satisfy the relation: D/C is 1.6 or more and the second region is located at a portion of the gate insulating material at a distance in a thickness direction of Y/10 of the gate insulating material from an interface between the channel region of the gate insulating material and the base.**

With regard to the range of D/C value recited (that is, D/C is 1.6 or more) at the portion of the gate insulating material at the distance in the thickness direction of Y/10 of the gate insulating material from the interface between the channel region of the gate insulating material and the base, the lower limited value (that is, 1.6) is supported by an example in the Applicant's specification (See Ex. 9 of Table 1). More particularly, as

shown in Table 1, the B/A value of Ex. 9 at the portion residing at the thickness direction of Y/10 of the gate insulating film from the interface is 1.6.

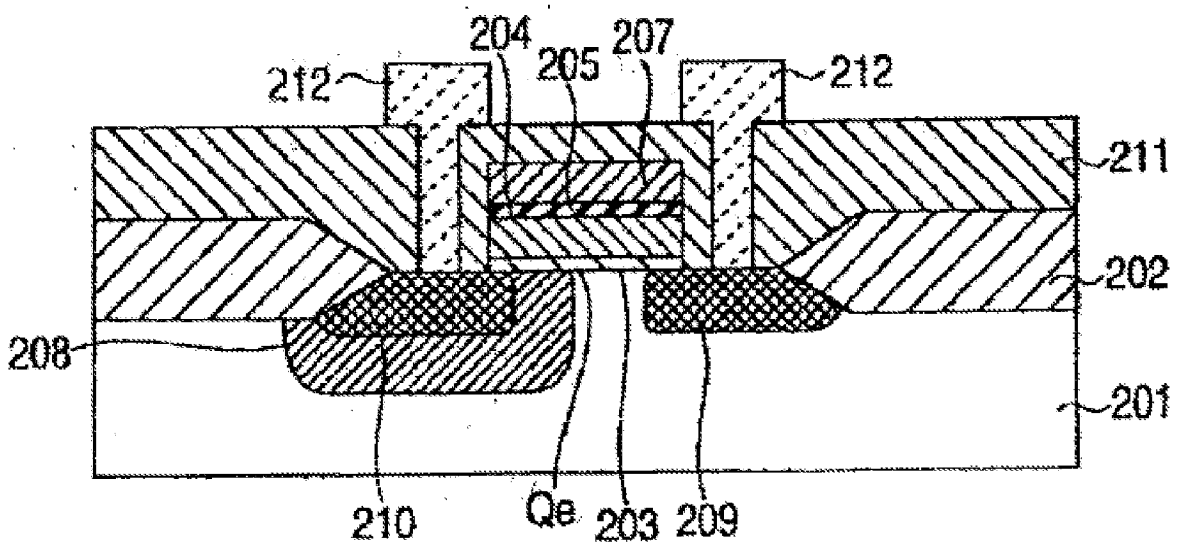
It is possible to reduce an absolute quantity of Si-OH structures in the vicinity of the interface of the gate insulating film formed from the gate insulating material as claimed when forming the gate insulating film by including the at least one other element (that is, at least one element other than the silicon, oxygen, hydrogen and deuterium), (Hereinbelow, the at least one other element is simple referred to as "the element X") in the insulating material (See lines 5-12 of page 16).

In the claimed invention, it is possible to reduce the amount of Si-OH structures that reside in the vicinity of the interface of the gate insulating film relatively (relative to one that does not contain the element X) and to prevent the Si-OH structures from increasing due to an external electric field by satisfying the relation recited in amended claim 1 so that resistance to the dielectric breakdown of the gate insulating film can be improved (See line 24 of page 16 to line 2 of page 17).

For anticipation to be present under 35 U.S.C §102(b), there must be no difference between the claimed invention and the reference disclosure as viewed by one skilled in the field of the invention. *Scripps Clinic & Res. Found. V. Genentech, Inc.*, 18 USPQ.2d 1001 (Fed. Cir. 1991). All of the limitations of the claim must be inherent or expressly disclosed and must be arranged as in the claim. *Constant v. Advanced Micro-Devices, Inc.*, 7 USPQ.2d 1057 (Fed. Cir. 1988). Here, Kobayashi et al. fails to disclose the configuration claim 1 recites.

More particularly, Kobayashi et al. discloses a flash memory provided with a memory cell array section in which a plurality of memory cells using the nonvolatile memory device (Qe) are provided as shown in Fig. 1 below.

FIG. 1



The nonvolatile memory device (Qe) of the flash memory of Kobayashi et al. comprises a p-type semiconductor substrate (201) used as a channel forming region, a first gate dielectric film (203), a floating gate electrode (204), a second gate dielectric film (205), a control gate electrode (207), a punch-through stopper region (208), a source region (209) and a drain region (210). Further, Kobayashi et al. discloses that the second gate dielectric film (205) contains silicon, oxygen, hydrogen and nitride wherein a nitrogen atomic concentration in the second gate dielectric film (205) is in the range of 2×10^{20} atoms/cm^3 to 2×10^{21} atoms/cm^3 and a hydrogen atomic concentration is 5×10^{20} atoms/cm^3. Therefore, in the case where the nitrogen atomic concentration

is defined as A is 2 x 10^{20} atoms/cm^3 and the hydrogen atomic concentration is defined as B is 5 x 10^{20} atoms/cm^3, the B/A value is 2.5.

However, **the second gate dielectric film (205)** of Kobayashi et al. **is disposed between the floating gate electrode (204) and the control gate electrode (207)** and is **not disposed in contact with the channel forming region of the substrate (201) like the claimed invention** (as shown in Fig. 1 above, the first gate dielectric film (203) is disposed in contact with the channel forming region of the p-type semiconductor substrate (201)). In addition, Kobayashi et al. does not disclose or suggest both a nitrogen atomic concentration and a hydrogen atomic concentration in the first gate dielectric film (203) disposed in contact with the channel forming region of the substrate (201). Therefore, Kobayashi et al. does not disclose the configuration of the claimed invention.

Inasmuch as the prior art fails to teach or suggest all of the claim limitations, the prior art cannot anticipate claim 1. Therefore, Applicant respectfully requests reconsideration and withdrawal of this rejection.

Claims 4-5, 10 and 13-14 depend from claim 1 and should be in condition for allowance for at least the same reasons as set forth above.

Applicant cancels claims 3 and 15.

REJECTION UNDER 35 U.S.C. § 103

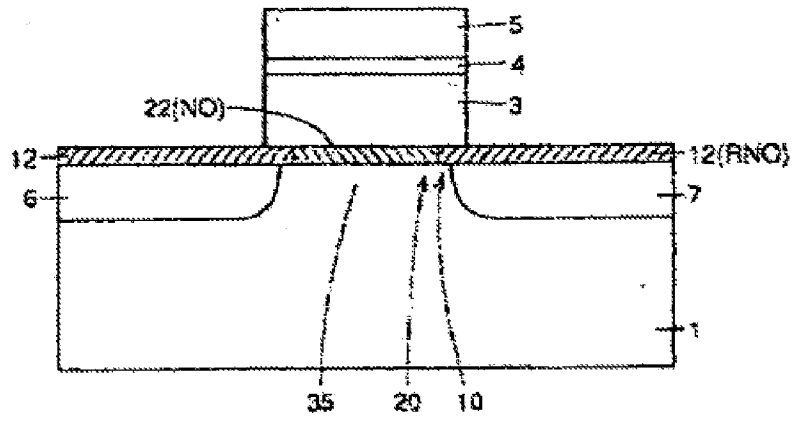
Claim 7 stands rejected under 35 U.S.C. § 103(a) as being unpatentable over Kobayashi et al. (U.S. Pat. No. 6,489,649). This rejection is respectfully traversed.

Claim 7 depends from claim 1 and should be in condition for allowance for at least the same reasons as set forth above.

Claims 1, 3-4, 7, 10, 13-14 and 15 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Kusunoki et al. (U.S. Pat. Pub. No. 2002/0066934). This rejection is respectfully traversed. It is a longstanding rule that to establish a prima facie case of obviousness of a claimed invention, all of the claim limitations must be taught or suggested by the prior art. *In re Royka*, 180 USPQ 143 (CCPA 1974), see MPEP §2143.03. Furthermore, when evaluating claims for obviousness under 35 U.S.C. §103, all of the limitations must be considered and given weight. *Ex parte Grasselli*, 231 USPQ 393 (Bd. App. 1983), MPEP § 2144.03. Here, Kusunoki et al. fails to teach or suggest the configuration of claim 1.

More particularly, Kusunoki et al. discloses a semiconductor device having a gate insulating film comprising RNO films (12) and a NO film (22) as shown in Fig. 1 below.

FIG. 1



The RNO films (12) are nitride oxide films which contain silicon, oxygen, and nitrogen at a content of 2.5 x 10^{20} /cm^3 or more and hydrogen at a content less than 3 x 10^{20} /cm^3. The NO film (22) is a nitride oxide film which contains silicon, oxygen, and

nitrogen at a content of 2.5 x 10^{20} /cm^3 or more and hydrogen at a content of 3 x 10^{20} /cm^3 or more.

In the case where the concentration of nitrogen in each of the films (the RNO films (12) and the NO film (22)) is defined as A and the concentration of hydrogen in each of the films is defined as B, the B/A value of each of the RNO films (12) is less than 1.2 as shown in below table. The value of 1.2 has been obtained based on the following values A and B.

	gate insulating film	
	NO film (22)	RNO film (12)
A	2.5×10^{20} /cm^3 or more	2.5×10^{20} /cm^3 or more
B	3×10^{20} /cm^3 or more	less than 3×10^{20} /cm^3
B/A	not identified	less than 1.2

Each of the RNO films (12) comprising the gate insulating film of Kusunoki et al. has a B/A value less than 1.2 throughout the RNO films (12) while the gate insulating film (gate insulating material) of the present invention has a D/C value of **1.6 or more at a distance in the thickness direction of Y/10 of the gate insulating material from an interface between the channel region of the gate insulating material and the base**. Since each of the RNO films (12) comprising the gate insulating film has a different composition from the gate insulating film (gate insulating material) than the claimed invention, the gate insulating film of Kusunoki et al., necessarily having the RNO films (12), is different from the gate insulating film (gate insulating material) of the claimed invention even if the NO film (22) has the same composition of the gate

insulating film (gate insulating material) of the claimed invention. Therefore, Kusunoki et al. cannot teach or suggest the configuration of the claimed invention.

Since Kusunoki et al. fails to teach or suggest all of the claim limitations, Kusunoki cannot render claim 1 unpatentable. Therefore, Applicant respectfully requests reconsideration and withdrawal of this rejection.

Claims 4, 7, 10 and 13-14 depend from claim 1 and should be in condition for allowance for at least the same reasons as set forth above.

Claims 3 and 15 are cancelled.

Claim 5 stands rejected under 35 U.S.C. § 103(a) as being unpatentable over Kusunoki et al. (U.S. Pat. Pub. No. 2002/0066934) in view of Hori et al. (U.S. Pat. No. 6,215,163). This rejection is respectfully traversed. Claim 5 depends from claim 1 and should be in condition for allowance for at least the same reasons as set forth above.

Claim 6 stands rejected under 35 U.S.C. § 103(a) as being unpatentable over Kobayashi et al. (U.S. Pat. No. 6,489,649) or Kusunoki et al. (U.S. Pat. Pub. No. 2002/0066934) in view of Mitani et al. (U.S. Pat. Pub. No. 2002/0140043). This rejection is respectfully traversed. Notwithstanding Applicant's traverse, Claim 6 is cancelled.

CONCLUSION

It is believed that all of the stated grounds of rejection have been properly traversed, accommodated, or rendered moot. Applicant therefore respectfully requests that the Examiner reconsider and withdraw all presently outstanding rejections. It is believed that a full and complete response has been made to the outstanding Office

Action and the present application is in condition for allowance. Thus, prompt and favorable consideration of this amendment is respectfully requested. If the Examiner believes that personal communication will expedite prosecution of this application, the Examiner is invited to telephone the undersigned at (248) 641-1600.

Respectfully submitted,

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